Field Effect Transistor Characterization

EE251 Laboratory Report #3

<name>

May 26, 2008

Abstract

The low frequency characteristics of the 2N7000 N channel MOS Transistor were measured and compared to published data for this transistor and the characterization of the transistor in PSpice using the published data. The characteristics found in the laboratory were found to be inconsistent with the data for reasons that are not yet understood.

1. Procedure

The 2N7000 transistor (TO-92 package version) was characterized in the Electronics Laboratory of Wilkes University using the circuit shown in Figure 1. The function generator used was the Tektronix model AGF 32022 Arbitrary Function generator; the power supply was the Aligent E3630A DC Power Supply, and the oscilloscope the Tektronix TDS2014. The signal generator was set to give its maximum sawtooth amplitude between zero and approximately 10 Volts. This particular signal generator can be operated with a floating ground (reference) which was particularly useful for this exercise. The DC Voltage at the gate was varied by changing the setting of the potentiometer R2, with the Voltage measured using a Jameco model JE110 Digital Multimeter. For four Voltages from 2.0 Volts to 4.0 Volts, the characteristic curve was displayed on the oscilloscope with the X axis (channel 1) being the drain Voltage, and the Y axis being the Voltage across R3 in the drain circuit, which was proportional to drain current. The polarity of the current measuring Voltage was reversed in order to render the normal display. Data from each curve were recorded for later analysis.

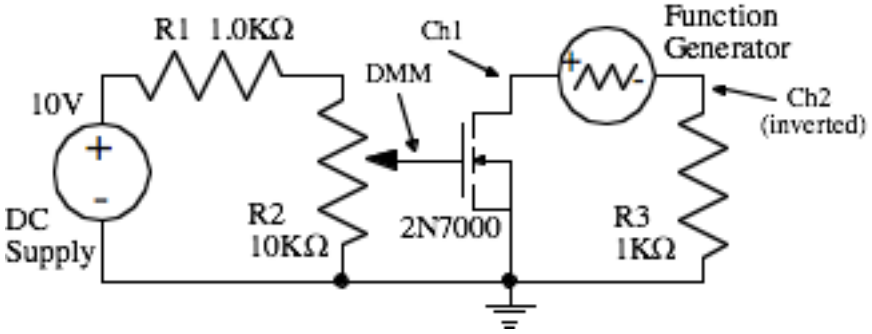

Figure 1 MOSFET Characterization Circuit

2. Results

The data recorded is given in Table 1. This data was derived from readings of the oscilloscope. the inverted channel 2 Voltage measurements for drain current, ID, were converted by dividing the Channel 2 Voltage by 1K Ohms to get currents in mA. Direct reading from the oscilloscope to a computer data file was not attempted because of the noise on the current readings. The tabulated data is plotted in Figure 2 as the transistor characteristic curves.

Table 1 Transistor characteristic data as observed

Gate Voltage (Volts)	Drain Voltage (Volts)	Drain Current (mAmperes)
1.5	for all	0.000
2.0	0.0	0.000
2.0	1.0	0.005
2.0	2.0	0.006
2.0	3.0	0.006
2.0	4.0	0.007
2.0	5.0	0.007
2.0	6.0	0.008
2.0	7.0	0.008
2.5	0.0	0.000
2.5	1.0	0.015
2.5	2.0	0.025
2.5	3.0	0.030
2.5	4.0	0.032
2.5	5.0	0.033
2.5	6.0	0.034
2.5	7.0	0.035
3.0	0.0	0.000
3.0	1.0	0.038
3.0	2.0	0.052
3.0	3.0	0.060
3.0	4.0	0.065
3.0	5.0	0.070
3.0	6.0	0.073
3.0	7.0	0.073
4.0	0.0	0.000
4.0	1.0	0.10
4.0	2.0	0.15
4.0	3.0	0.18
4.0	4.0	0.20
4.0	5.0	0.20
4.0	6.0	0.20
4.0	7.0	0.20

The desired characteristics of the transistor are V_{TN}, the gate turn-on Voltage, and K_n, the parameter that characterizes the drain current as a function of Gate Voltage V_{GS}. The relationship for the saturated region, where $V_{GS} < V_{DS}$, is given in Equation 1 (Jaeger and Blalock):

$$I_D = (K_n /2) (V_{GS} - V_{TN})^2 \quad (1)$$

In order to estimate the values of these parameters, the square root of I_D was plotted against V_{GS}, as shown in Figure 3, giving what should be a straight line.

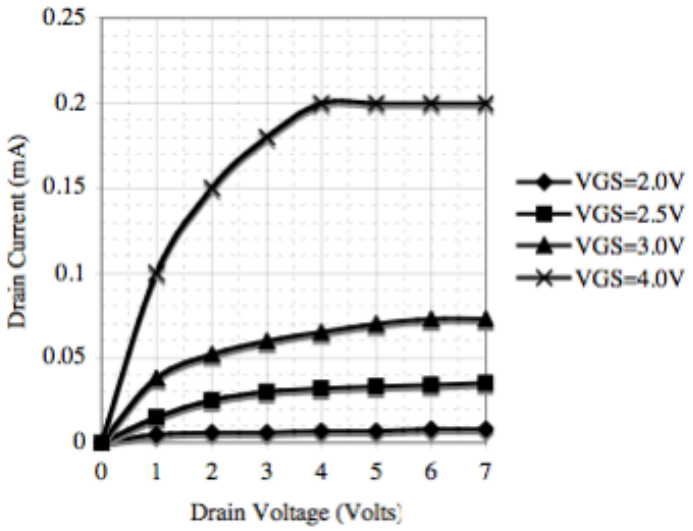

Figure 2 Observed transistor Characteristics

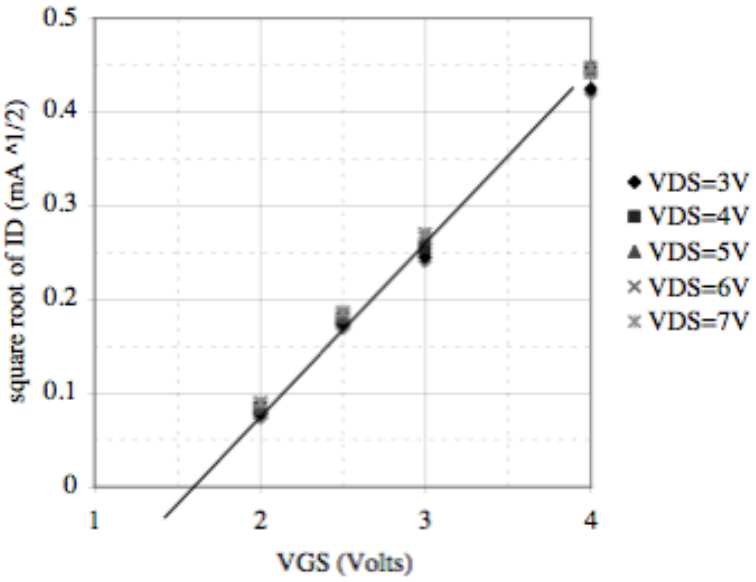

Figure 3 Plot of square root of drain current versus gate Voltage for saturated region

Using Figure 3 it is found that V_{TN} is about 1.6 Volts. The line was calculated to have an average slope of 0.179 $mA^{½}/V$. For each point an x intercept was calculated. Averaging all of these gives V_{TN}=1.52, assumed to be closer than the graphical estimate. Kn was calculated for each point in the saturated region (V_{DS} = 3V or more) using this V_{TN} value and the corresponding I_D and V_{GS} using Equation 2. The numbers averaged, to give K_n=.054mA/V^2.

$$K_n = 2\, I_D /(V_{GS} - V_{TN})^2 \qquad (2)$$

The values for I_D for the largest V_{GS} showed little fluctuation in the saturated region, suggesting that any attempt to find λ, the rate of change of I_D with respect to V_{DS}, are suspect. The slope if I_D from V_{DS} = 3V to 7 V was used to calculate a supposed value for Lambda using Equation 3.

$$\lambda_{est} = (I_{DVGS=7V} - I_{DVGS=3V})/(4V\ I_{DVGS=3V}) \qquad (3)$$

The four values were quite different, .08, .04, .05, and .03 V^{-1} respectively, for each of the four different V_{GS} values. The values for lower V_{GS} were more affected by noise, but the last value may be too large from inclusion of the point at V_{DS}=3V, which isn't quite in the saturated region. A reasonable guess based on these results would be about .04 V^{-1}, with poor accuracy. Had V_{DS} been larger or the data better, the estimate would be improved by using the projected I_D at V_{GS}=0 in the denominator.

3. Modeling

The "Student" version of PSpice does not have the 2N7000 part in its library, so the generic NMOS transistor "MBreakN" was modified to match. The key parameters found on the data sheet are shown in Table 2 (Fairchild). Because of the wide range of possible values for V_{TN} (given as $\mathbf{V_{GS(th)}}$), the value from the characterization above, 1.52V, was used. Equation 3, for transconductance given drain current, was solved to find a K_n of 90 mA/V^2 for the typical transconductance at .5A of .3S.

$$g_m = \text{sqrt}\ (2\ I_D\ K_n) \qquad (3)$$

Table 2 Key parameters from Data Sheet

$\mathbf{V_{GS(th)}}$	Gate Threshold Voltage	Minimum .3Volts, Maximum 3.9 Volts at V_{DS}=V_{GS}, I_D=250μA Minimum .4Volts, Maximum 2.2 Volts at V_{DS}=V_{GS}, I_D=1mA
$\mathbf{g_{fs}}$	Forward transconductance	Minimum .1 S, typical .3S at V_{DS}=15V, I_D=.5A

A PSpice circuit was constructed as shown in Figure 4, and the parameters set to represent the characteristics of the 2N7000: VTO 1.52 KP 90mA LAMBDA .04 A simulation run was performed as a DC sweep with V2 varied from 0V to 7V in .01V increments, and V1 varied from 2.0 to 4.0 Volts in .5 Volt increments, corresponding to the laboratory tests performed. The results are shown in Figure 5. While the general shape of the curves is not far different from that produced from the experimental data, the current scale is far different, bu three orders of magnitude.

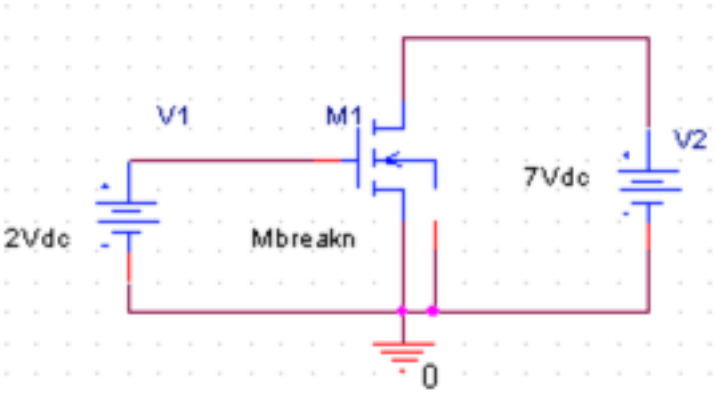

Figure 4 PSpice circuit for generating characteristic curves

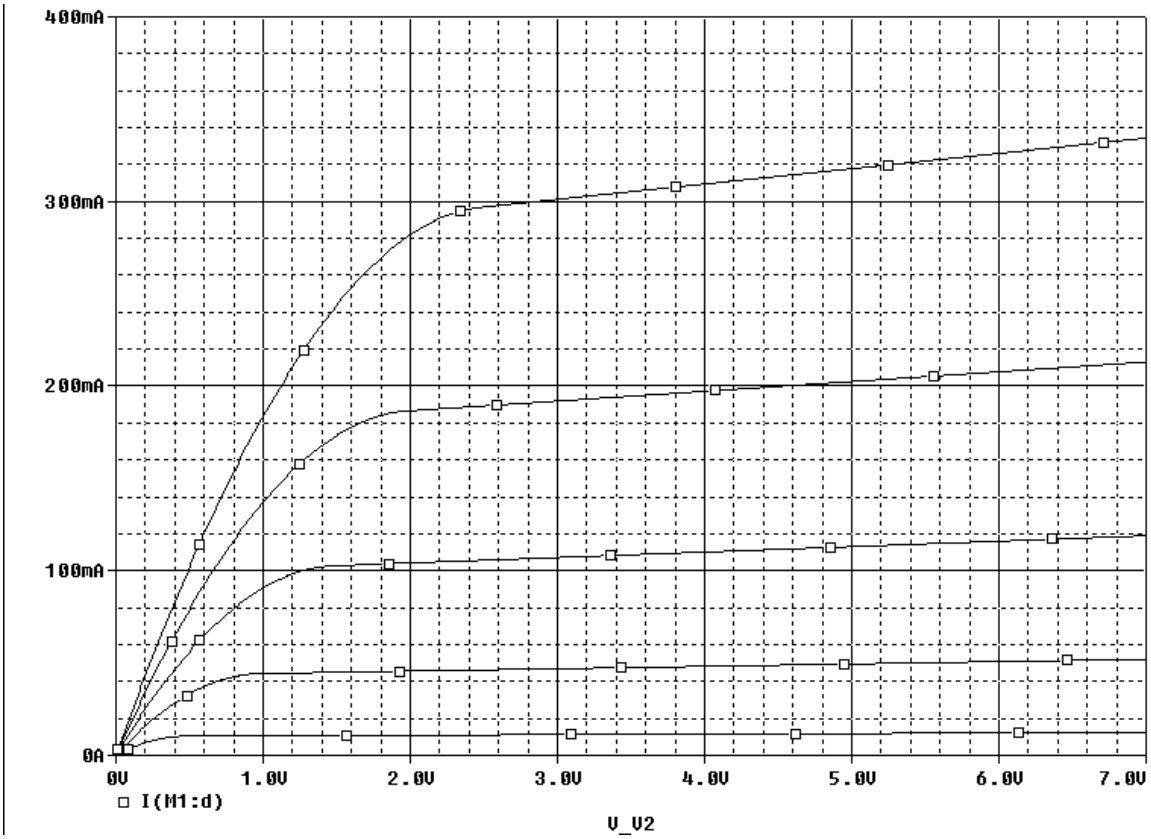

Figure 5 Characteristic curves generated by PSpice using datasheet Kn

A second PSpice run was made using instead the K_n value of .054 mA / V^2 derived from the data taken in the laboratory. The same values were used vor the other PSpice parameters. The set of curves generated is shown in Figure 6. These curves indeed correspond fairly closely to the laboratory data as expected, although the top curve is not as flat as the lab data showed. (Also, note that these curves include the missing trace for V_{GS} = 3.5 V, a setting that was not used in the laboratory.)

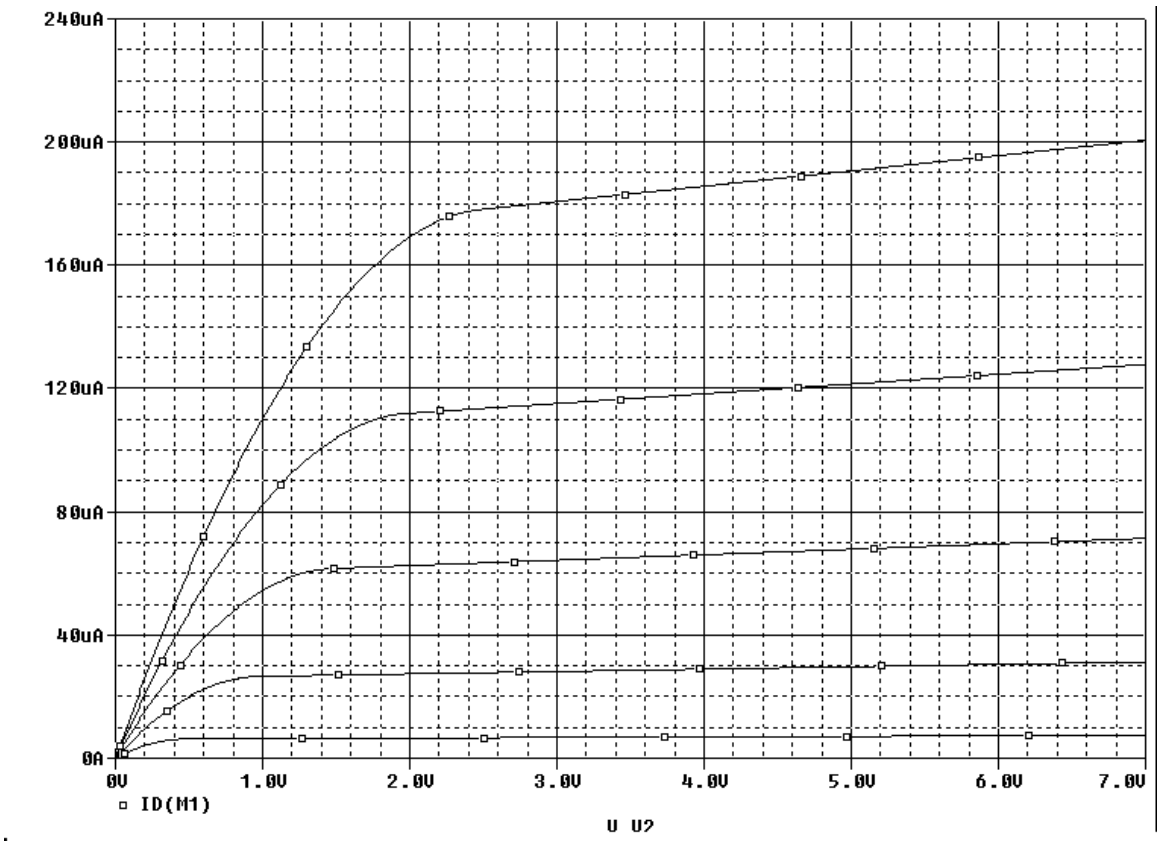

Figure 6 Characteristic curves using Experimentally determined Kn

4. Conclusions

The laboratory exercise was successful in producing characteristic curves for the 2N7000 transistor, but the current scale for these curves, and the value of Kn found, differ greatly from those of the device data sheet. The difference is about three orders of magnitude. This is outside the bounds of device variations that can be expected. Thus, it is not possible to escape the conclusion that some error was made in the experimental procedure. Some of the possibilities include:

1. The oscilloscope scaling was incorrect for the probe for Channel 2. However, the probes have at most a multiplier of x10, so at worst this would result in currents off by one order of magnitude, not three.

2. The currents were incorrectly written down as mA where they should actually have been in Amperes. However, the largest current would then be .2 Amperes which would cause too large of a Voltage drop to allow a datum for the point at V_{GS}=4V, V_{DS}=7V.

3. The transistor may have suffered static or some other kind of damage. However, this should have been apparent from a nonlinear scaling of the V_{GS} values with potentiometer setting, and such an effect was not noticed.

At this time, this lab exercise must be regarded as a failure, producing inexplicable results. It needs to be repeated, and the source of the error found. It would also be useful to

repeat the PSpice runs using the full version found in the laboratories at Wilkes University, which included the 2N7000 part, and see if it is consistent with the data sheet values. Unfortunately, at this writing that version is unavailable due to a licensing process failure.

Acknowledgements

Thanks is due to Thomas Wychock and Jack Hosford, whose report from EE251 in 2008 was a source for much of the data included in this sample lab report (Wychock). The original lab exercise was more extensive, including some other measurements and transistors.

References

Fairchild Semiconductor, "Small Signal MOSFET 2N7000BU/2N7000TA", accessed from http://www.jameco.com/Jameco/Products/ProdDS/1201672.pdf on 26 May, 2008.

Jaeger, Richard C. and Blalock, Travis N., *Microelectronic Circuit Design*, 3rd ed., McGraw Hill, New York, 2008, p154.

Thomas Wychock, "EE 251 Electronics 1 Laboratory, Experiment #3, Field Effect Transistors," Wilkes University, 25 February, 2008.

Remarks:

This is an example of what to do when the experiment fails. The calculated value of Kn was so far off that there was no chance that this was just a random variation; there must have been some error. It is not obvious exactly what the error was. However, the lab report is due. So, in the conclusions, one can only state what has happened as forthrightly as possible, explain or suggest possible sources of the problem, and if no explanation can be found, recommend that the exercise be repeated.

One other thing to note here is the fact that for the Excel graphs, the fonts and font sizes were selected to match the document. The colors were changed to monochrome and grey scale. Quite a bit of manipulation was needed for each of these graphs. The PSpice circuit was pasted in with no special care (the colored lines are dark enough to print satisfactorily in monochrome), but the two PSpice graphs were originally white and green (or red) on black. For a report, graphs should be black on white. So, the original images captured from the screen were copied into an image manipulation program, *Photostudio* (which came with a Canon MP800 printer), and the negative was taken and then thresholded and saved as a PICT file, which was then inserted into Word. (A JPEG or PNG might be more preferable now.)

In this particular report, the modeling followed the experiment procedure and results sections, because the modeling was used as an analysis tool, for verification. If modeling is used as a design step, the simulation development and discussion might be better placed ahead of the laboratory procedure and results.